AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An interleaver for a turbo encoder in a Universal Mobile Telecommunications System (UMTS) ~~an UMTS~~, comprising:

a register for updating and registering a plurality of parameters for setting an operating condition of the interleaver;

an address calculator for generating a finally interleaved address using an inter-row permutation pattern T(j), an intra-row permutation pattern increment arrangement value incr(j) and an intra-row permutation basic sequence s(i) provided from the register; and

a data storage device for storing data input to the turbo encoder and outputting data corresponding to the address generated by the address calculator.

2. (Original) The interleaver as claimed in claim 1, wherein the address calculator comprises:

an intra-row permutation pattern generator for calculating an intra-row permutation pattern value using the intra-row permutation pattern increment arrangement value incr(j);

an intra-row permutation pattern storage arrangement device for storing intermediate data while the intra-row permutation pattern generator calculates the intra-row permutation pattern; and

a final address generator for calculating an address of finally interleaved data using the inter-row permutation pattern T(j) from the register and the intra-row permutation basic sequence s(i) corresponding to the intra-row permutation pattern value generated by the intra-row permutation pattern generator.

3. (Original) The interleaver as claimed in claim 1, wherein the register updates and registers parameters used to calculate inter-row/intra-row permutation pattern of the input data to be interleaved, and provides the parameters to an intra-row permutation pattern generator of the address calculator to generate an intra-row permutation pattern for generating an interleaved final intra-row permutation pattern.

4. (Original) The interleaver as claimed in claim 1, wherein the register updates and registers a parameter K indicating a number of input data bits; a parameter μ indicating a primitive root; a parameter p indicating a prime number; a parameter R indicating a number of rows of the input data; a parameter C indicating a number of columns of the input data; and a parameter TypeD indicating an exceptional process request signal, wherein the parameters are used to calculate the inter-row permutation pattern T(j); the intra-row permutation pattern increment arrangement value incr(j); and the intra-row permutation basic sequence s(i).

5. (Original) The interleaver as claimed in claim 2, wherein the intra-row permutation pattern generator uses an inter-row inverse permutation pattern TI(j) determined by inversing the inter-row permutation pattern T(j) to calculate a permuted prime integer sequence r(j) for calculating a final intra-row permutation pattern $U^j(i)$.

6. (Original) The interleaver as claimed in claim 2, wherein the intra-row permutation pattern generator comprises:

a first adder for adding a previous intra-row permutation pattern read from an intra-row permutation pattern memory of the register with the intra-row permutation pattern increment arrangement value incr(j) to thereby output a first add value;

a second adder for adding the first add value output from the first adder to a prime number -(p-1) to thereby output a second add value;

a first multiplexer for selectively outputting one of the first and second add values from the first and second adders;

a sign detector connected to the second adder and the first multiplexer for providing a selection control signal to the first multiplexer so that the first multiplexer outputs the second add value as an address of the intra-row permutation basic sequence s(i) when the second add value has a positive value, and outputs the first add value as an address of the intra-row permutation basic sequence when the second add value has a negative value; and

a second multiplexer for outputting a predetermined initial value during an initial operation of the intra-row permutation pattern generator, and then providing the output of the

first multiplexer as a read address of the intra-row permutation pattern storage arrangement device for a succeeding intra-row permutation pattern.

7. (Original) The interleaver as claimed in claim 1, wherein the increment arrangement value incr(j) is calculated in accordance with a following equation:

$$incr(j) = r\{TI(j)\} \bmod (p-1)$$

where incr(j): increment,

TI(j): inter-row inverse permutation pattern,

p: prime number, and

r(j): permuted prime integer sequence.

8. (Original) The interleaver as claimed in claim 6, wherein the intra-row permutation pattern storage arrangement device sequentially stores a read address of one column output from the second multiplexer, and feeds back a previously stored read address to the first adder.

9. (Original) The interleaver as claimed in claim 1, wherein the data is input sequentially to the data storage device.

10. (Currently Amended) A method for performing interleaving in an interleaver for a turbo encoder, comprising the steps of:

permuting an inter-row address of input data according to an intra-row ~~inter-row~~ permutation pattern T(j) determined depending on a number of input data bits;

calculating an increment incr(j) for generating an intra-row ~~inter-row~~ permutation pattern a(j) using the permuted inter-row address;

calculating an intra-row permutation pattern using the increment incr(j) and a previous intra-row permutation pattern; and

calculating a read address of an intra-row permutation basic sequence s(i) for permuting an intra-row address of the input data using the intra-row permutation pattern.

11. (Original) The method as claimed in claim 10, further comprising the steps of:

calculating a final intra-row permutation pattern;

calculating a finally interleaved address using the final intra-row permutation pattern and the inter-row permutation pattern T(j); and

sequentially outputting data corresponding to the finally interleaved address thereby interleaving the input data.

12. (Original) The method as claimed in claim 10, further comprising the step of sequentially storing the data input to the turbo encoder in a data memory.